

LGaDB65R150N

650V GaN enhancement mode power transistor datasheet

1.Features

- 650 V enhancement mode power transistor
- $R_{DS(on)} = 150\text{m}\Omega(\text{max.})@V_{GS}=6\text{V}$
- $I_{DS}(\text{max, Pulse})=36\text{A}$
- Simple gate drive requirements(-10V to 7 V)
- Very high switching frequency
- Fast and controllable fall and rise times
- Reverse conduction capability
- Zero reverse recovery loss
- Reliable and rugged

2.Applications

- AC_DC Converters
- DC_DC Converters
- Bridgeless Totem Pole PFCs
- Inverters
- Energy Storage Systems
- Solar Energy
- On Board Chargers
- Uninterruptable Power Supplies
- Appliances
- Motor & Pump Drives
- Laser Drivers

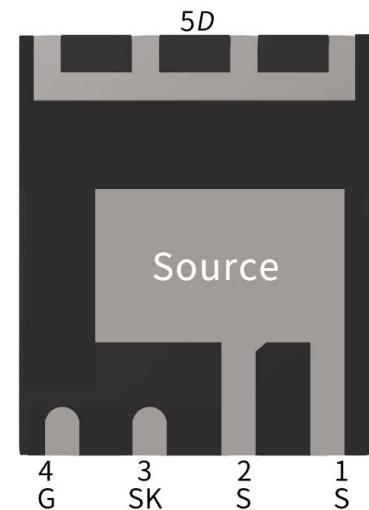
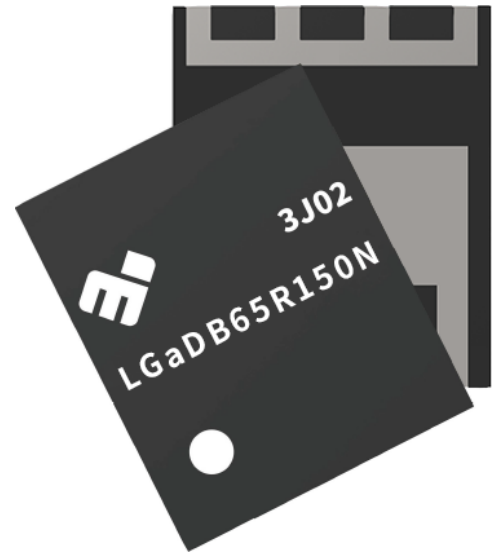
3.Description

The LGaDB65R150N is an enhancement mode GaN-on-QST(Qromis Substrate Technology) power transistor.

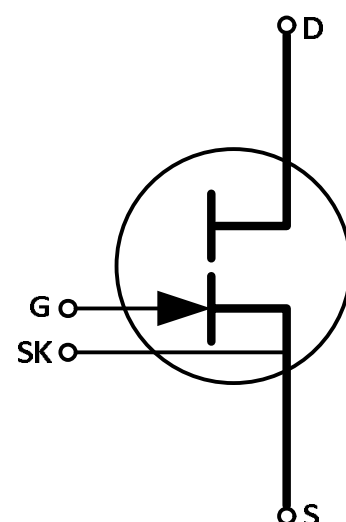
The QST substrate provides a path for achieving a very thick GaN buffer layer, making the device more suitable for high voltage and high current application scenarios.

The properties of GaN allow for high current, high voltage breakdown and high switching frequency.

The LGaDB65R150N offers very low junction-to-case thermal resistance for demanding high power applications. These features combine to provide very high efficiency power switching.



Gate	4
Drain	5
Kelvin Source	3
Source	1,2



Absolute Maximum Ratings ($T_{case} = 25\text{ }^{\circ}\text{C}$ except as noted)

Parameter	Symbol	Value	Unit
Operating Junction Temperature	TJ	-55 to +150	$^{\circ}\text{C}$
Storage Temperature Range	TS	-55 to +150	$^{\circ}\text{C}$
Drain-to-Source Voltage	VDS	650	V
Drain-to-Source Voltage – transient (Note 1)	VDS(transient)	850	V
Gate-to-Source Voltage	VGS	- 10 to +7	V
Gate-to-Source Voltage – transient (Note 1)	VGS(transient)	-20 to +10	V
Continuous Drain Current ($T_{case} = 25\text{ }^{\circ}\text{C}$)	IDS	18	A
Continuous Drain Current ($T_{case} = 100\text{ }^{\circ}\text{C}$)	IDS	12	A
Pulse Drain Current (Pulse width 10 μs , VGS = 6 V) (Note 2)	IDS Pulse	36	A

(1) For $\leq 1\text{ }\mu\text{s}$

(2) Defined by product design and characterization. Value is not tested to full current in production.

Thermal Characteristics (Typical values unless otherwise noted)

Parameter	Symbol	Value	Units
Thermal Resistance (junction-to-case) – bottom side	R θ JC	1.34	$^{\circ}\text{C}/\text{W}$
Thermal Resistance (junction-to-ambient) (Note 3)	R θ JA	39	$^{\circ}\text{C}/\text{W}$
Maximum Soldering Temperature (MSL3 rated)	TSOLD	260	$^{\circ}\text{C}$

(3) Device mounted on 1.6 mm PCB thickness FR4, 4-layer PCB with 2 oz. copper on each layer. The recommendation for thermal vias under the thermal pad is 0.3 mm diameter (12 mil) with 0.635 mm pitch (25 mil). The copper layers under the thermal pad and drain pad are 25 x 25 mm² each. The PCB is mounted in horizontal position without air stream cooling.

Electrical Characteristics (Typical values at $T_J = 25\text{ }^{\circ}\text{C}$, $V_{GS} = 6\text{ V}$ unless otherwise noted)

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Drain-to-Source Blocking Voltage	$V_{(BL)DSS}$	650			V	$V_{GS} = 0\text{ V}$, $I_{DSS} \leq 18\text{ }\mu\text{A}$
Drain-to-Source On Resistance	$R_{DS(on)}$		140	150	m Ω	$V_{GS} = 6\text{ V}$, $T_J = 25\text{ }^{\circ}\text{C}$ $I_{DS} = 3.2\text{ A}$
Gate-to-Source Threshold	$V_{GS(th)}$	1.3	1.9	2.6	V	$V_{DS} = V_{GS}$, $I_{DS} = 2.4\text{ mA}$
Gate-to-Source Current	I_{GS}		180		μA	$V_{GS} = 6\text{ V}$, $V_{DS} = 0\text{ V}$
Gate Plateau Voltage	V_{plat}		3.1		V	$V_{DS} = 400\text{ V}$, $I_{DS} = 6\text{ A}$
Drain-to-Source Leakage Current	I_{DSS}		7	18	μA	$V_{DS} = 650\text{ V}$, $V_{GS} = 0\text{ V}$ $T_J = 25\text{ }^{\circ}\text{C}$
Drain-to-Source Leakage Current	I_{DSS}		23		μA	$V_{DS} = 650\text{ V}$, $V_{GS} = 0\text{ V}$ $T_J = 150\text{ }^{\circ}\text{C}$
Internal Gate Resistance	R_G		1.5		Ω	$f = 5\text{ MHz}$
Input Capacitance	C_{ISS}		156		pF	$V_{DS} = 400\text{ V}$ $V_{GS} = 0\text{ V}$ $f = 100\text{ kHz}$
Output Capacitance	C_{OSS}		40		pF	
Reverse Transfer Capacitance	C_{RSS}		0.6		pF	
Effective Output Capacitance, Energy Related (Note 4)	$C_{O(ER)}$		56		pF	$V_{GS} = 0\text{ V}$ $V_{DS} = 0\text{ to }400\text{ V}$
Effective Output Capacitance, Time Related (Note 5)	$C_{O(TR)}$		76		pF	
Total Gate Charge	Q_G		3.8		nC	$V_{GS} = 0\text{ to }6\text{ V}$ $V_{DS} = 400\text{ V}$ $I_{DS} = 6\text{ A}$
Gate-to-Source Charge	Q_{GS}		1.5		nC	
Gate-to-Drain Charge	Q_{GD}		1.1		nC	
Output Charge	Q_{OSS}		30		nC	$V_{GS} = 0\text{ V}$, $V_{DS} = 400\text{ V}$
Reverse Recovery Charge	Q_{RR}		0		nC	

(4) $C_{O(ER)}$ is the fixed capacitance that would give the same stored energy as C_{OSS} while V_{DS} is rising from 0 V to the stated V_{DS} .

(5) $C_{O(TR)}$ is the fixed capacitance that would give the same charging time as C_{OSS} while V_{DS} is rising from 0 V to the stated V_{DS} .

Electrical Characteristics cont'd (Typical values at $T_J = 25\text{ }^{\circ}\text{C}$, $V_{GS} = 6\text{ V}$ unless otherwise noted)

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Turn-On Delay	$t_{D(on)}$		8		ns	$V_{DD} = 400\text{ V}$, $V_{GS} = 0\text{-}6\text{ V}$, $I_{DS} = 6\text{ A}$, $R_{G(on)} = 15\text{ }\Omega$, $R_{G(off)} = 2\text{ }\Omega$, $L = 300\text{ }\mu\text{H}$, $LP = 9\text{ nH}$ (Notes 6,7,8)
Rise Time	t_R		9		ns	
Turn-Off Delay	$t_{D(off)}$		10		ns	
Fall Time	t_F		8.5		ns	
Switching Energy during turn-on	E_{on}		32		μJ	
Switching Energy during turn-off	E_{off}		6.5		μJ	
Output Capacitance Stored Energy	E_{OSS}		4.5		μJ	$V_{DS} = 400\text{ V}$ $V_{GS} = 0\text{ V}$, $f = 100\text{ kHz}$

(6) See Figure 16 for switching test circuit diagram.

(7) See Figure 17 for switching time definition waveforms.

Electrical Performance Graphs

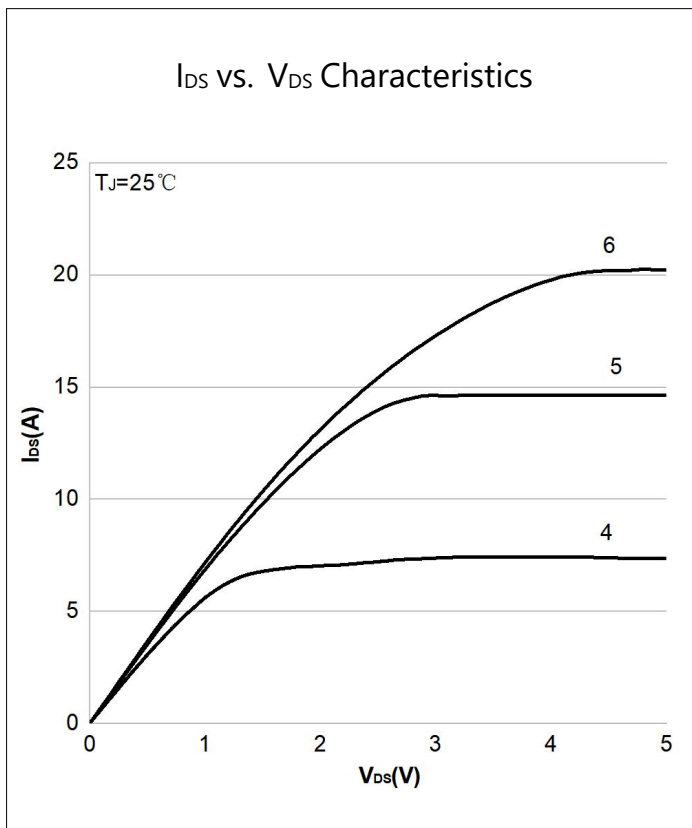


Figure 1: Typical I_{DS} vs. V_{DS} @ $T_J = 25^\circ\text{C}$

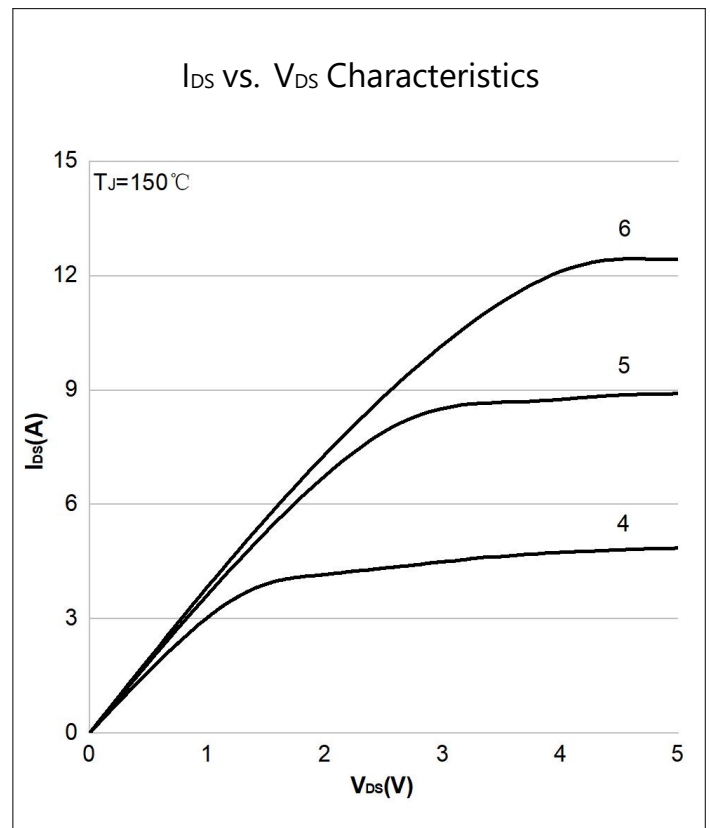


Figure 2: Typical I_{DS} vs. V_{DS} @ $T_J = 150^\circ\text{C}$

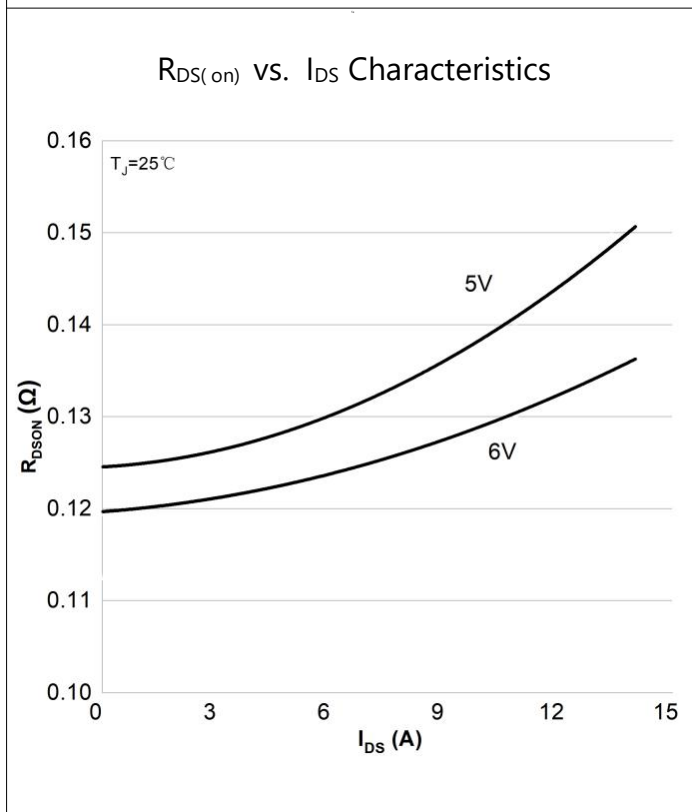


Figure 3: $R_{DS(on)}$ vs. I_{DS} at $T_J = 25^\circ\text{C}$

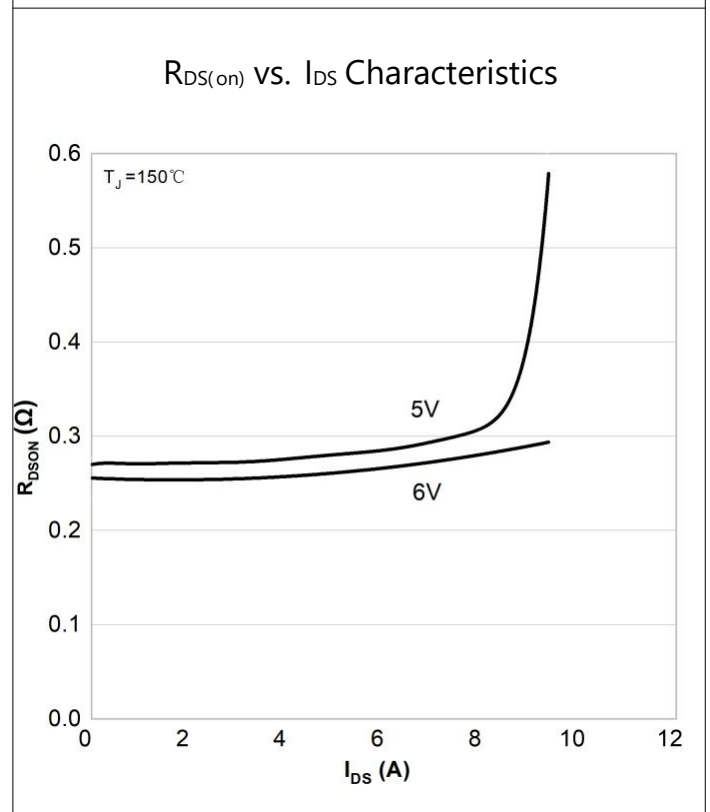


Figure 4: $R_{DS(on)}$ vs. I_{DS} at $T_J = 150^\circ\text{C}$

Electrical Performance Graphs

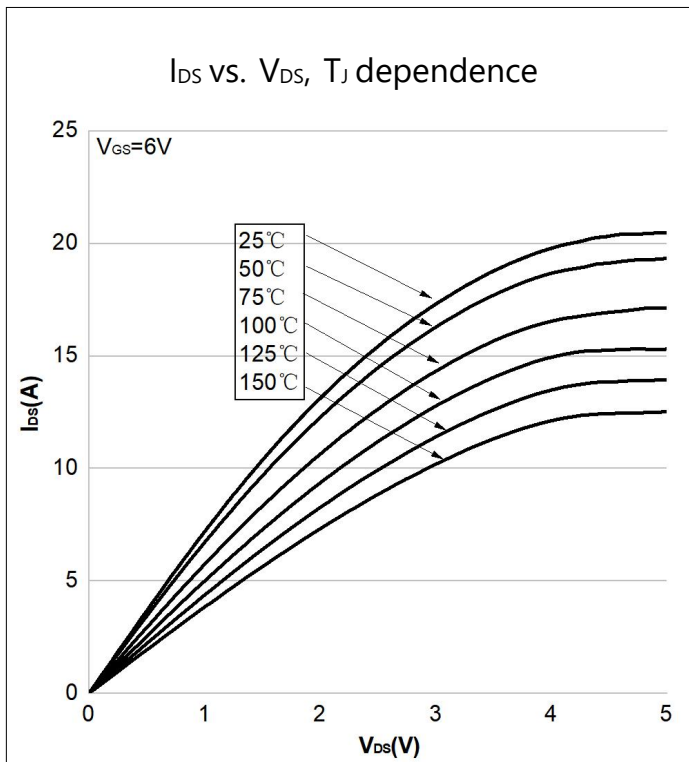


Figure 5: Typical I_{DS} vs. V_{DS} @ $V_{GS} = 6V$

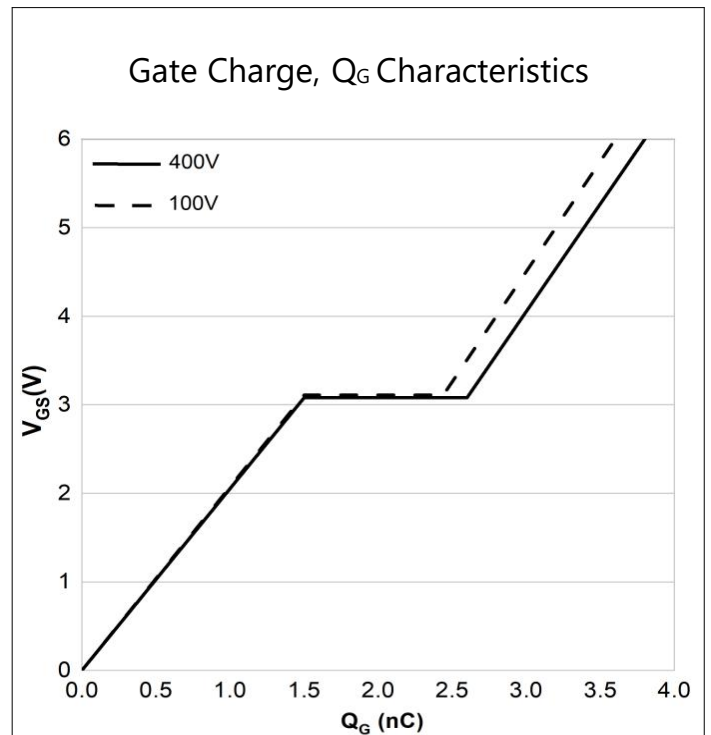


Figure 6: Typical V_{GS} vs. Q_G @ $V_{DS} = 100, 400V$

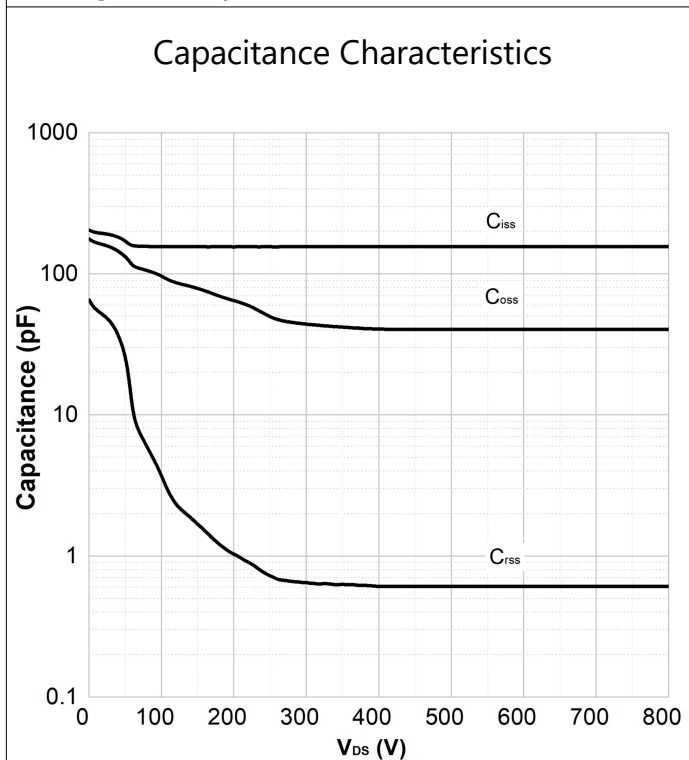


Figure 7: Typical C_{iss} , C_{oss} , C_{rss} vs. V_{DS}

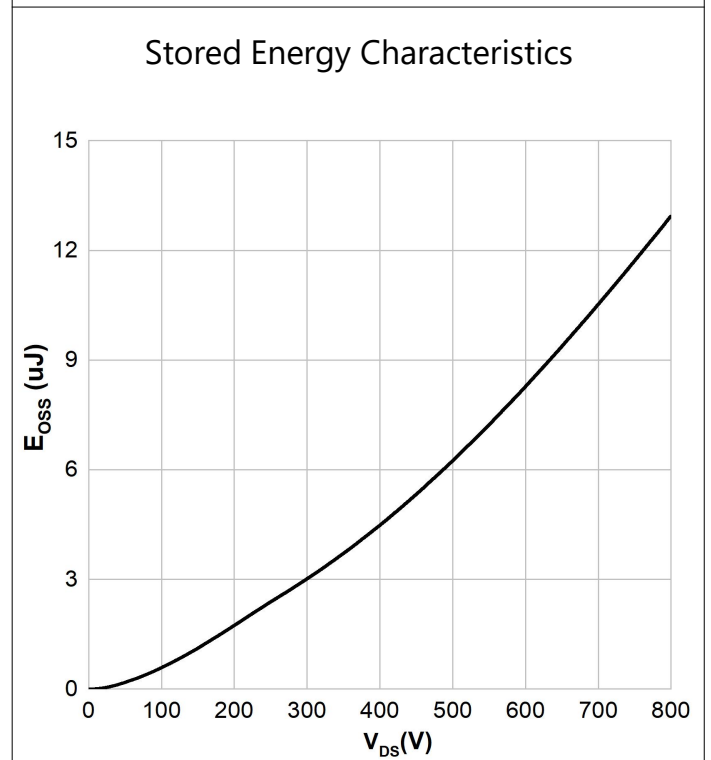


Figure 8: Typical C_{oss} Stored Energy

Electrical Performance Graphs

Reverse Conduction Characteristics

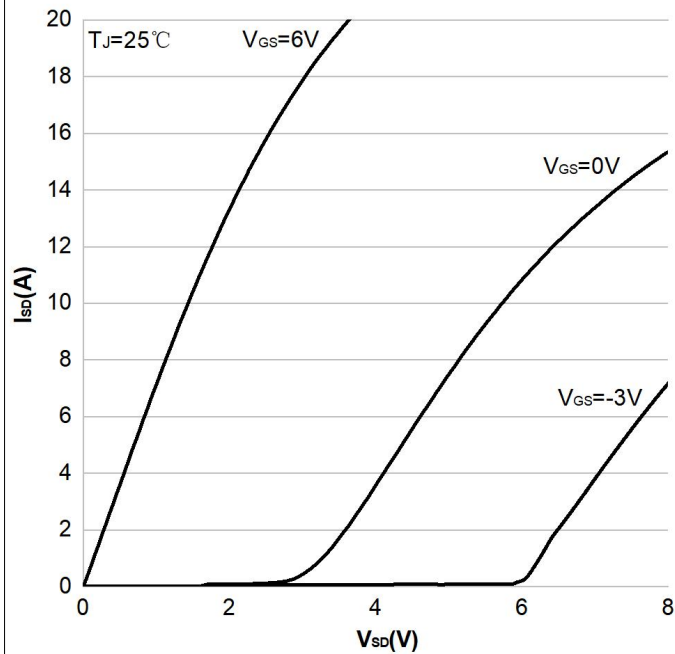


Figure 9: Typical I_{SD} vs. V_{SD} @ $T_J = 25\text{ }^{\circ}\text{C}$

Reverse Conduction Characteristics

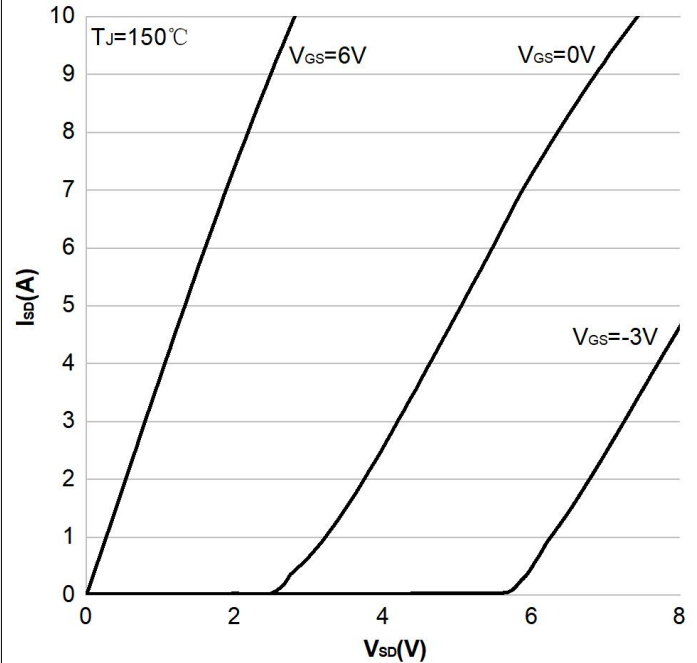


Figure 10: Typical I_{SD} vs. V_{SD} @ $T_J = 150\text{ }^{\circ}\text{C}$

I_{DS} vs. V_{GS} Characteristics

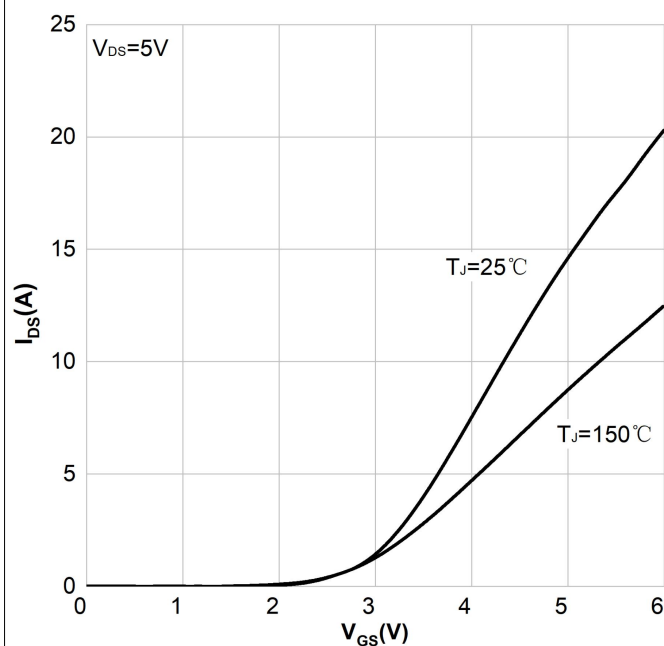


Figure 11: Typical I_{DS} vs. V_{GS}

$R_{DS(on)}$ Temperature Dependence

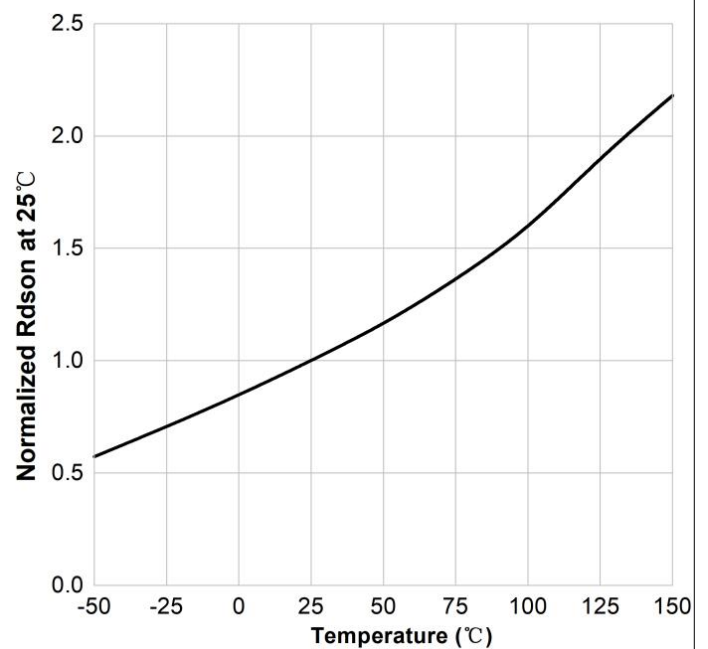


Figure 12: Normalized $R_{DS(on)}$ as a function of T_J

Thermal Performance Graphs

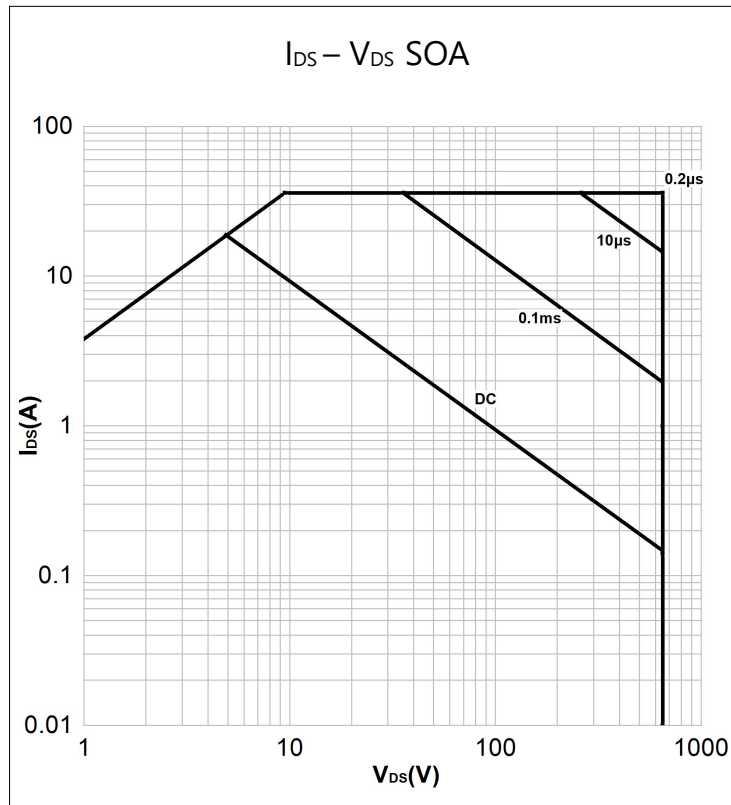


Figure 13: Safe Operating Area @ $T_{case} = 25^\circ\text{C}$

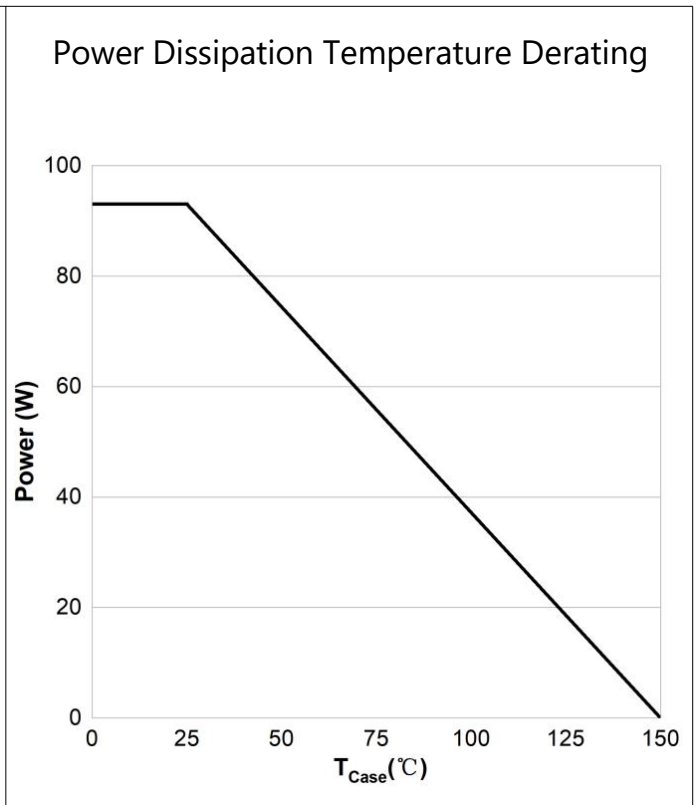


Figure 14: Power Derating vs. T_{case}

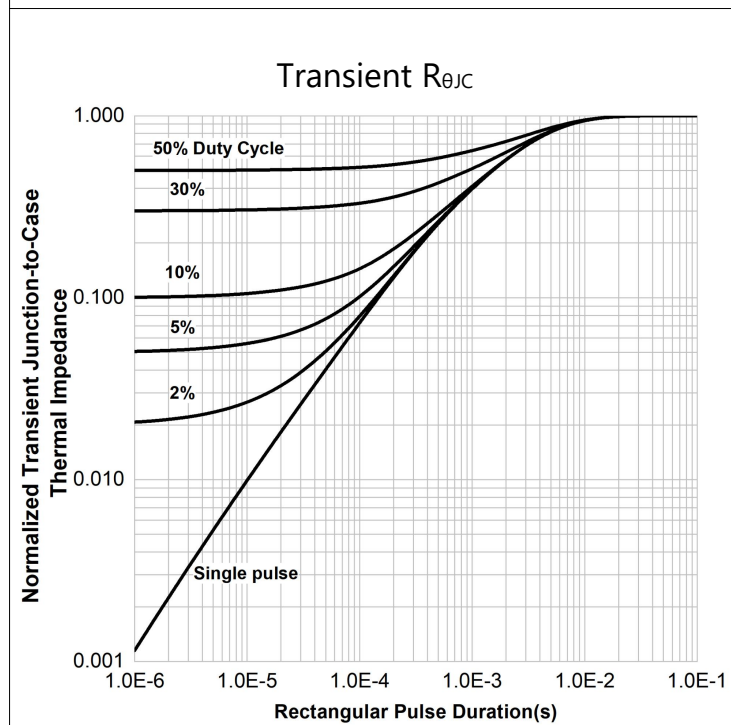


Figure 15: Transient Thermal Impedance

(1.00 = Nominal DC thermal impedance)

Test Circuits

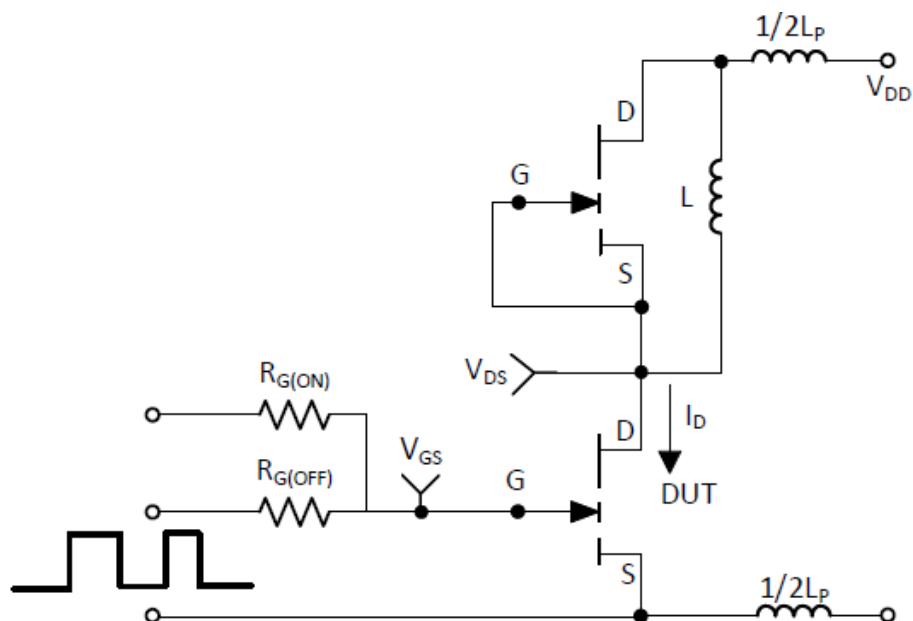


Figure 16: Switching Test Circuit

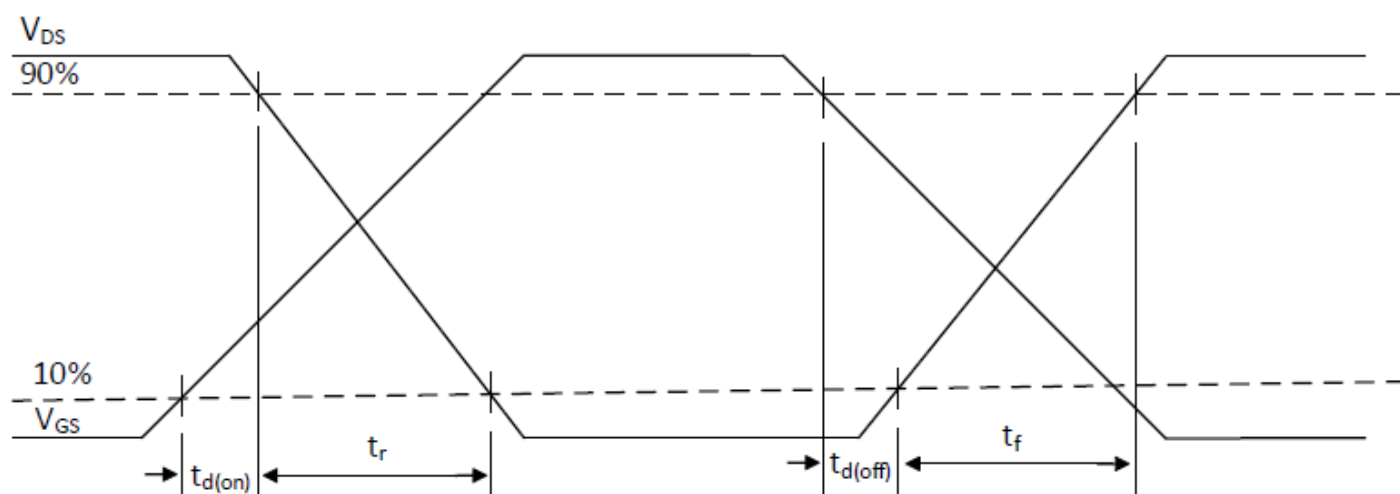


Figure 17: Switching Time Waveforms

DIMENSION	MILLOMETERS		
	MIN	NOM	MAX
A	—	0.750	1.350
A1	—	0.050	—
b	0.475	0.500	0.525
D	4.900	5.000	5.100
D1	4.297	4.300	4.330
E	5.900	6.000	6.100
E1	2.165	2.200	2.235
E2	4.265	4.300	4.335
e	1.245	1.270	1.295
K1	0.870	0.895	0.920
K2	1.475	1.500	1.525
L	0.675	0.700	0.725
f	0.325	0.350	0.375
H	0.325	0.350	0.375
h	0.675	0.700	0.725
g	0.275	0.300	0.325

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