LGMA100DQ2

High-frequency and high-performance quasi-resonant mode AC-DC power switch integrated with QST GaN HEMT

Features

- AC-DC power switch integrated 650V QST GaN HEMT and drive adjustment function
- Integrated high-voltage start-up and X-capacitor discharge function
- Ultra-low starting and working current, standby power consumption < 30mW
- The highest working frequency can be adjusted in three steps (500kHz, 300kHz, 140kHz) in bottom locking mode
- Ultra-wide VDD power supply range 9V-112V
- Integrated EMI optimization technology
- Built-in protection functions:
  - VDD over/undervoltage protection (VDD OVP/UVLO)
  - Output overvoltage protection (OVP)
  - Input overvoltage/Brown-out protection (LOVP/BOP)
  - Built-in overtemperature protection (OTP)
  - Cycle-by-cycle overcurrent protection limit (COCP)
  - Overload protection (OLP)
  - Abnormal overcurrent protection (AOCP)
  - CS pin open circuit protection

Applications

- Fast charger and adapter
- Set-top Box, Digital Photo Frame
- Auxiliary power supply of Server, PC, Printer, TV
- Home theater/Audio System, White Goods

Descriptions

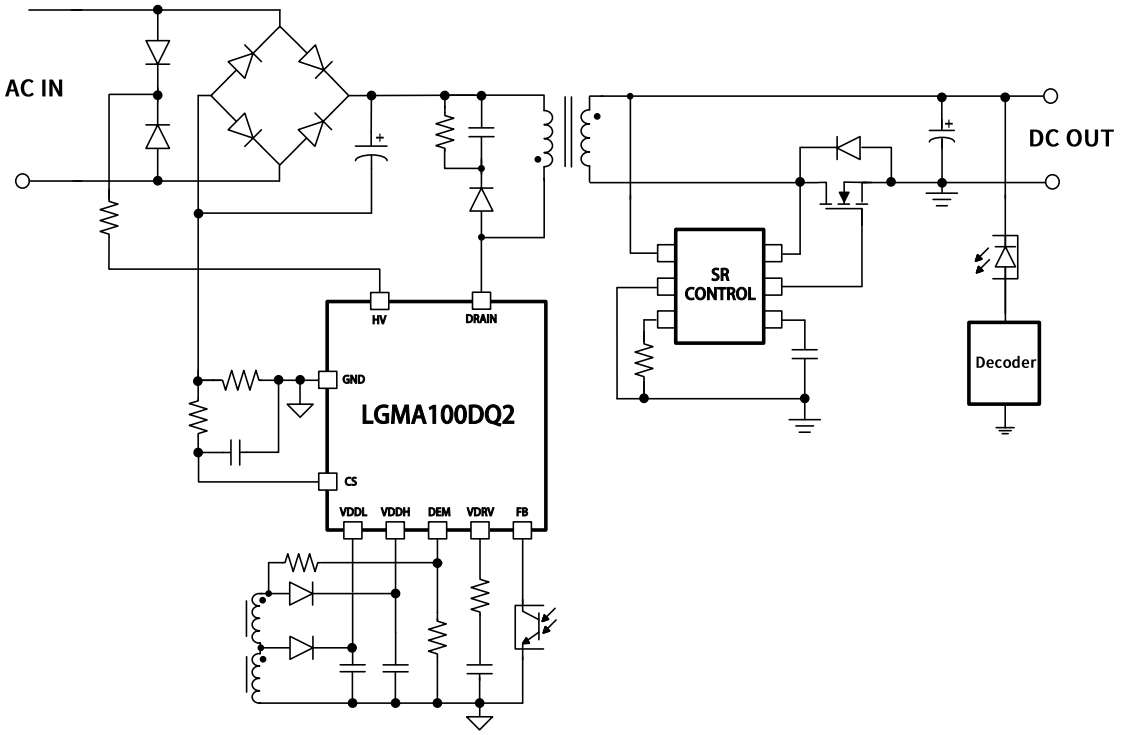
LGMA100DQ2 is a high-frequency and high-performance quasi-resonant mode AC-DC power switch integrated with QST GaN HEMT. The chip integrates drive adjustment function, which can adjust the driving speed when GaN HEMT is turned on and optimize the EMI performance of the system.

The LGMA100DQ2 features quasi-resonant (QR) operation. QR control improves efficiency by reducing switching loss and benefits EMI performance with natural frequency variation, and an internal frequency limitation is utilized to overcome the inherent disadvantages of QR Flyback.

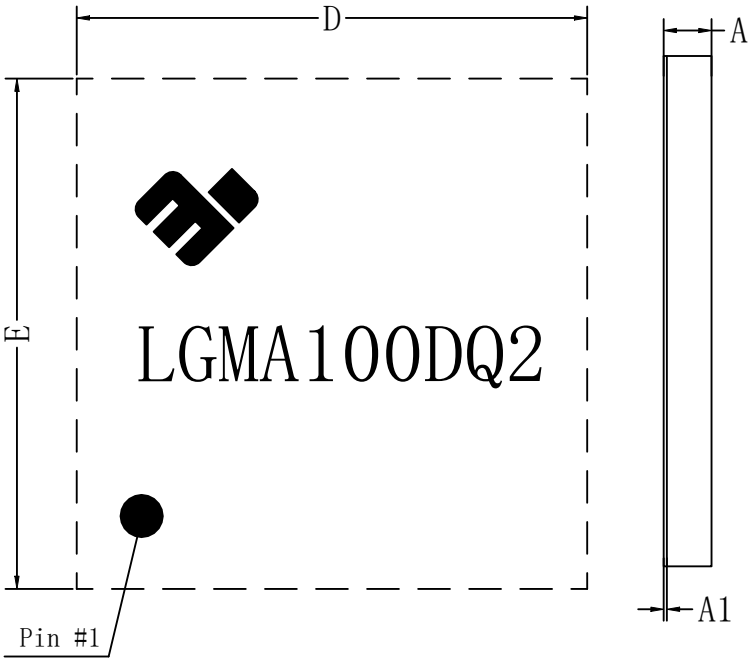
The operating frequency of LGMA100DQ2 is up to 500kHz, and it can work in a quasi-resonant mode in a full range. The chip supports ultra-wide VDD range of 9V-112V. The chip comprises a HV pin for startup to eliminate conventional startup resistor and save standby mode energy consumption. Also, the HV pin is used for X-cap discharge when AC input is removed, which helps to reduce X-cap discharge loss and achieve extremely low standby power loss of less than 30mW.

LGMA100DQ2 is packaged in a small DFN 8x8mm package, which is suitable for the design of AC/DC converters with high frequency and high power density and wide input/output range.

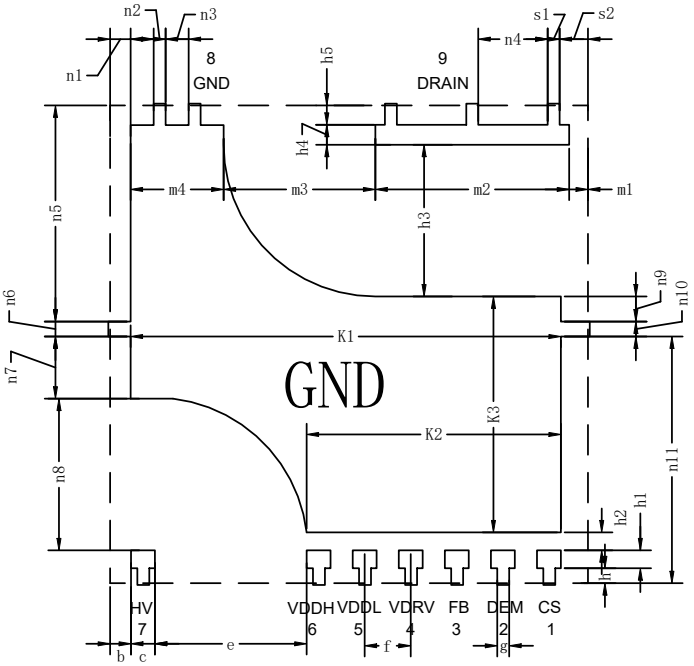
Typical application circuit diagram



Package information



正面



背面

DIMENSION	MILLOMETERS		
	MIN	NOM	MAX
A	–	0.750	1.350
A1	–	0.050	–
b	0.320	0.350	0.380
c	0.370	0.400	0.430
D	7.970	8.000	8.030
E	7.970	8.000	8.030
e	–	2.540	–
f	0.741	0.771	0.801
g	0.170	0.200	0.230
h	0.220	0.250	0.280
h1	0.270	0.300	0.330
h2	0.270	0.300	0.330
h3	–	2.540	–
h4	0.305	0.335	0.365
h5	0.295	0.325	0.355

DIMENSION	MILLOMETERS		
	MIN	NOM	MAX
K1	7.153	7.203	7.253
K2	4.226	4.256	4.286
K3	3.921	3.951	3.981
m1	0.284	0.314	0.344
m2	3.215	3.245	3.275
m3	–	2.540	–
m4	1.527	1.557	1.587
n1	0.313	0.343	0.373
n2	0.170	0.200	0.230
n3	0.356	0.386	0.416
n4	1.132	1.162	1.192
n5	3.590	3.620	3.650
n6	0.220	0.250	0.280
n7	1.010	1.040	1.070
n8	–	2.540	–

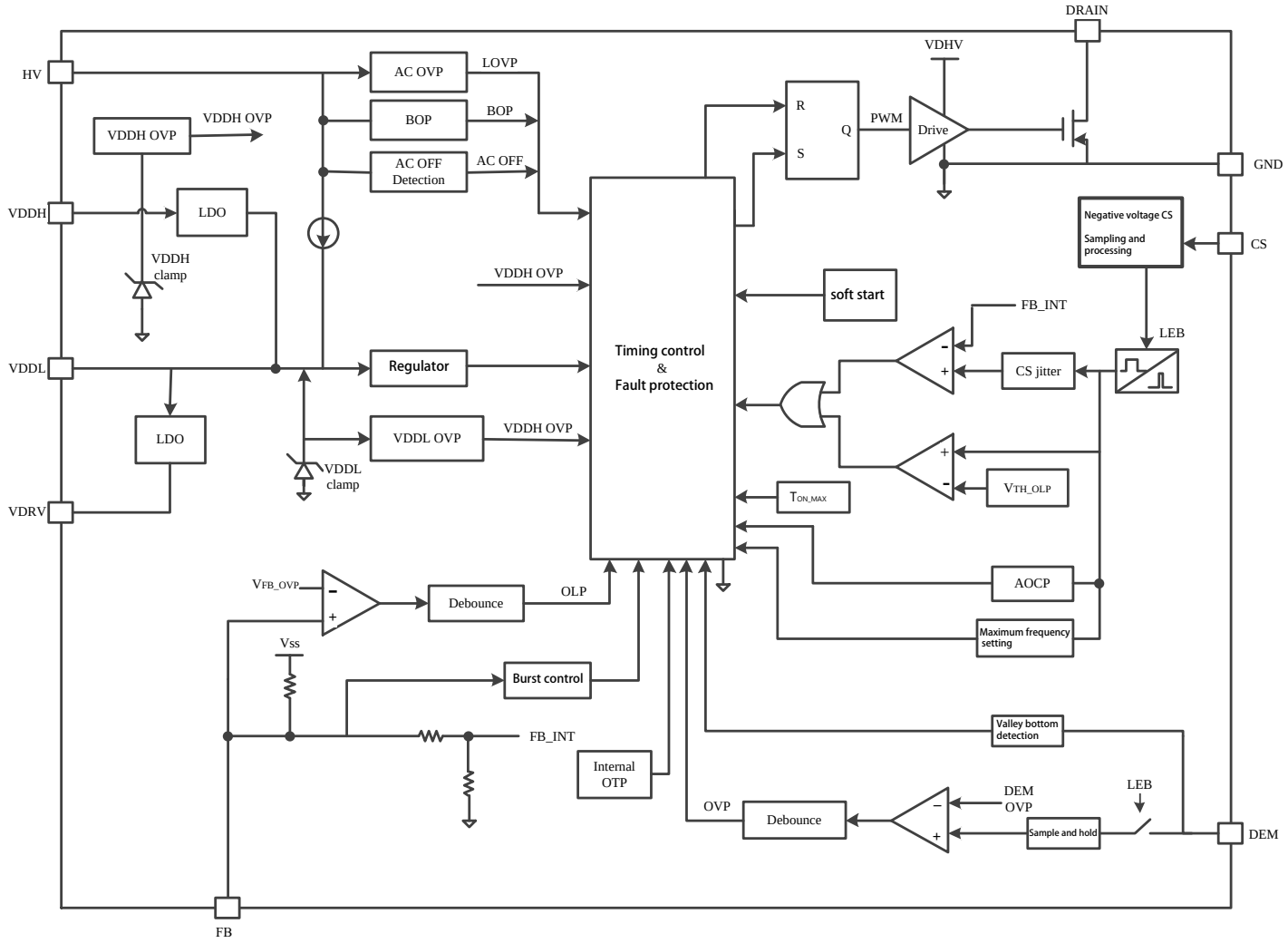
DIMENSION	MILLOMETERS		
	MIN	NOM	MAX
n9	0.391	0.421	0.451
n10	0.220	0.250	0.280
n11	4.100	4.130	4.160
n12	–	2.540	–
s1	0.170	0.200	0.230
s2	0.444	0.474	0.504

Pin definition and description

Pin number	Name	Type(1)	Description
1	CS	I/O	Current sampling input,multiplexing the highest frequency selection function.
2	DEM	I	Multifunctional pin, including transformer demagnetization detection, output OVP detection, etc.
3	FB	I	Feedback input pin connected to the photoelectric coupler.
4	VDRV	I/O	The external voltage-stabilizing port of GaN HEMT driving circuit, and external resistor for adjusting the driving turn-on rate.
5	VDDL	P	Low voltage VDD power supply pin, also the output end of built-in high voltage LDO, power supply for the chip.
6	VDDH	P	High voltage VDD power supply pin, also the input end of built-in high voltage LDO.
7	HV	P	High-voltage start-up pin, with over-voltage protection of input voltage and discharge function of X capacitor at the same time.
8	GND	P	High voltage GaN HEMT chip reference ground, Source of high voltage GaN HEMT
9	DRAIN	P	High voltage GaN HEMT drain

Note: (1) I is the input port, I/O is the input/output port and P is the power port.

Internal functional block diagram



Absolute Maximum parameter (2)

Parameter	Limit values	Unit
HV voltage	-0.3 to 700	V
DRAIN voltage	-0.3 to 650	V
VDDH supply voltage	-0.3 to 120	V
VDDH clamping current	10	mA
VDDL supply voltage	-0.3 to 30	V
FB,DEM voltage	-0.3 to 6	V
CS voltage	-6 to 6	V
Maximum working junction temperature of chip	150	℃
Storage temperature range	-65 to 150	℃
Welding temperature (10s)	260	℃
ESD Human Body Model (HBM)(3)	±4	kV
ESD charging device model (CDM)(4)	±2	kV

(2) Exceeding the limit parameters in the list may cause permanent damage to the chip. The chip may not work properly if it exceeds the recommended working conditions. Excessive exposure beyond the recommended working conditions may affect the reliability of the chip.
(3) The chip meets the requirements of HBM ESD at 500V level according to JEP155.
(4) The chip meets the requirements of CDM ESD at 250V level according to JEP155.

Recommended working conditions

Parameter	Limit values	Unit
VDDH supply voltage	15 to 100	V
VDDL supply voltage	10 to 26	V
Working junction temperature of chip	-40 to 125	℃

Electrical parameters (T_A=25℃,V_{VDDH}=18V,Unless otherwise stated.)

Symbol	Parameter	Test condition	Min	Typical	Max	Unit
High voltage starting part (HV pin)						
I_{HV}	High voltage startup current	V_{HV}=40V V_{VDDL}=V_{DD_ON}	1		2.5	mA
I_{HV_LKG}	High voltage leakage current	V_{HV}=700V	50		300	μA
		V_{VDDL}=18V				
V_{BOP}	AC Brown-out protection trigger threshold			70		V_{AC}
V_{BOP_HYS}	AC Brown-out protection recovery threshold			77		V_{AC}

T_{BOP_DELAY}	AC Brown-out protection confirmation time(5)			100		ms
V_{LOVP}	AC OVP trigger threshold			315		V_{AC}
T_{LOVP_DELAY}	AC OVP protection confirmation time(5)			130		ms
T_{DET}	Input power failure detection time			47		ms
T_{SET}	Confirm discharge timing			47		ms
T_{DIS}	Single discharge duration			47		ms
I_{DIS}	discharging current			5		mA
Power supply part (VDD pin)						
$V_{VDDH\ OVP}$	VDDH OVP threshold			112		V
V_{VDDH_CLAMP}	VDDH clamp voltage	I_{VDDH}=7mA		118		V
V_{VDDL_START}	VDDL startup current			70		μA
V_{VDDL_OP}	VDDL work current	V_{FB}=2V		1		mA
V_{VDDH_DIS}	VDDH active discharge current	V_{VDDH} > 20V		2		mA
V_{VDDL_on}	VDDL turn-on current			13		V
V_{VDDL_off}	VDDL turn-off current			6.8		V
$V_{VDDL\_HV\_CLAMP}$	Clamping voltage of VDDL HV power supply			7.8		V
V_{VDD_ERROR}	Fault confirmation time of VDDL continuous HV power supply			80		ms
V_{VDDL_REQ}	VDDH supply voltage to VDDL			12.5		V
V_{VDDL_OVP}	VDDL OVP threshold			28		V
V_{VDDL_CLAMP}	VDDL clamp voltage	I_{VDDL}=7mA		30		V
Feedback part (FB pin)						
V_{FB_OPEN}	FB open circuit			5.2		V
I_{FB_SHORT}	FB short circuit current			175		μA
V_{SKIP_IN}	FB threshold for entering Burst mode			0.5		V
$V_{SKIP\_OUT\_MIN}$	Minimum threshold for exiting Burst mode(5)			0.6		V
$V_{SKIP\_OUT\_MAX}$	Maximum threshold for exiting Burst mode(5)			0.9		V
V_{TH_OLP}	FB voltage threshold of overload protection			3.2		V
T_{OLP_DELAY}	Overload protection delay time(5)			75		ms

Electrical parameters (T_A=25℃,V_{VDDH}=18V,Unless otherwise stated.)

Symbol	Parameter	Test condition	Min	Typical	Max	Unit
Current sampling part (CS pin)						
T_{LEB}	Leading edge blanking time(5)			250		ns
V_{CS_MAX}	Overcurrent protection threshold	T_{ON} > 4μs		-0.6		V
		T_{ON} < 1.5μs		-0.5		V
V_{CS_AOCP}	Abnormal overcurrent protection threshold			-0.9		V
N_{AOCP}	AOCP blanking period number(5)			3		Cycle
V_{CS_MIN}	Minimum CS peak voltage			-0.15		V
T_{D_DELAY}	Turn-off delay of overcurrent protection(5)			70		ns
V_{OCP_SEC}	Output overcurrent protection threshold	V_{DEM} > 1.6V		265		mV
		V_{DEM} < 1.5V		390		mV
T_{OCP_SEC}	Delay time of triggering output overcurrent protection(5)			180		ms
F_{S_MAX}	highest frequency	R_{SEL}=400Ω		480		kHz
		R_{SEL}=1.2KΩ		300		kHz
		R_{SEL}=2KΩ		140		kHz
Multifunctional pin (DEM pin)						
V_{TH_OVP}	Output voltage overvoltage threshold			3.6		V
N_{OVP_TRIQ}	Trigger OVP protection timing(5)			6		Cycle
V_{TH_ZCD}	Zero crossing detection threshold			50		mV
$V_{TH\_ZCD\_HYS}$	Zero crossing detection hysteresis			30		mV
Overtemp protection part						
T_{SD}	Built-in thermal shutdown threshold(5)			150		℃
T_{RC}	Built-in overheat recovery threshold(5)			125		℃
GaN drive voltage part (DRV pin)						
V_{DRV}	Voltage for Gan drive circuit			6.2		V

Electrical parameters (T_A=25℃,V_{VDDH}=18V,Unless otherwise stated.)

Symbol	Parameter	Test condition	Min	Typical	Max	Unit
Time sequence						
$T_{\_SHUFFLE}$	Peak current jitter period(5)			500		μS
$\triangle I_{pk}/I_{px}$	Peak current jitter(5)	V_{AC}＞160V_{AC}		±8		%
		V_{AC}＜160V_{AC}		±4		%
T_{REC}	Restart time after triggering protection(5)			1.3		s
T_{ST}	Soft start time			4		ms
T_{ON_MAX}	Maximum on-time			20		μs
F_{S_BURST}	Minimum frequency of burst			22		kHz
F_{S_MIN}	Lowest frequency			10		kHz

(5) The parameters depend on the design and pass the functional test in mass production.

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